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Inorganic Materials COMMENTARY

Recent research of possible strategies on data-intensive processing

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Data-intensive computing and processing have stimulated strategies study for integrated circuits (IC). Some key factors including precision and reliability need to be systematically considered and verified to evaluate the abilities and feasibilities of the strategies proposed for present data processing including artificial intelligence (AI) neural network training, signal processing in wireless communications and differential equation solving in scientific computing. In order to solve the issues of data-intensive computing and processing, mainly four ways could be proposed, i.e., materials, devices, architectures, and algorithms (MDAA), and discussed. This bottom-up framework of MDAA spans from hardware foundations to software optimizations, with many materials form devices, many devices constitute architectures and the software improvement following the above hardware improvement, aiming at presenting a logically coherent and conceptually rigorous research. Among them, improvement of devices emerges as a particularly critical pathway.

MATERIALS

Materials are a critical direction for advancing data-intensive processing strategies. On one hand, 3D materials (notably Si) have dominated ICs for decades due to mass-producibility and high stability, laying the foundation for traditional data processing. On the other hand, the information era's demand for massive data processing (e.g., AI) has accelerated IC advancement, spurring research into new devices and materials. Materials are investigated because semiconductor devices are materials-based. For example, two-dimensional (2D) materials have attracted attention due to their different properties from the dominant 3D materials, particularly after graphene's Nobel Prize recognition. Extensive research has been performed, aiming to solve the issues such as variability and instability that the industry believes need to be addressed before any real and prompt applications on practical devices, including improving processing and transferring techniques to the samples based on the Si foundry.[1-3]

There are advantages such as the ultrathin thickness of 2D materials, which could be in a molecular dimension. However, the practical uses of 2D materials remain great challenges, including the inadequate long-term stability of many 2D materials with properties that severely hinder their practical applications.[1,2] In consideration of these, considerable research on the 2D materials role in adapting the semiconductor foundry process chips remains an open topic, and it might have hopes if the improved methods could be

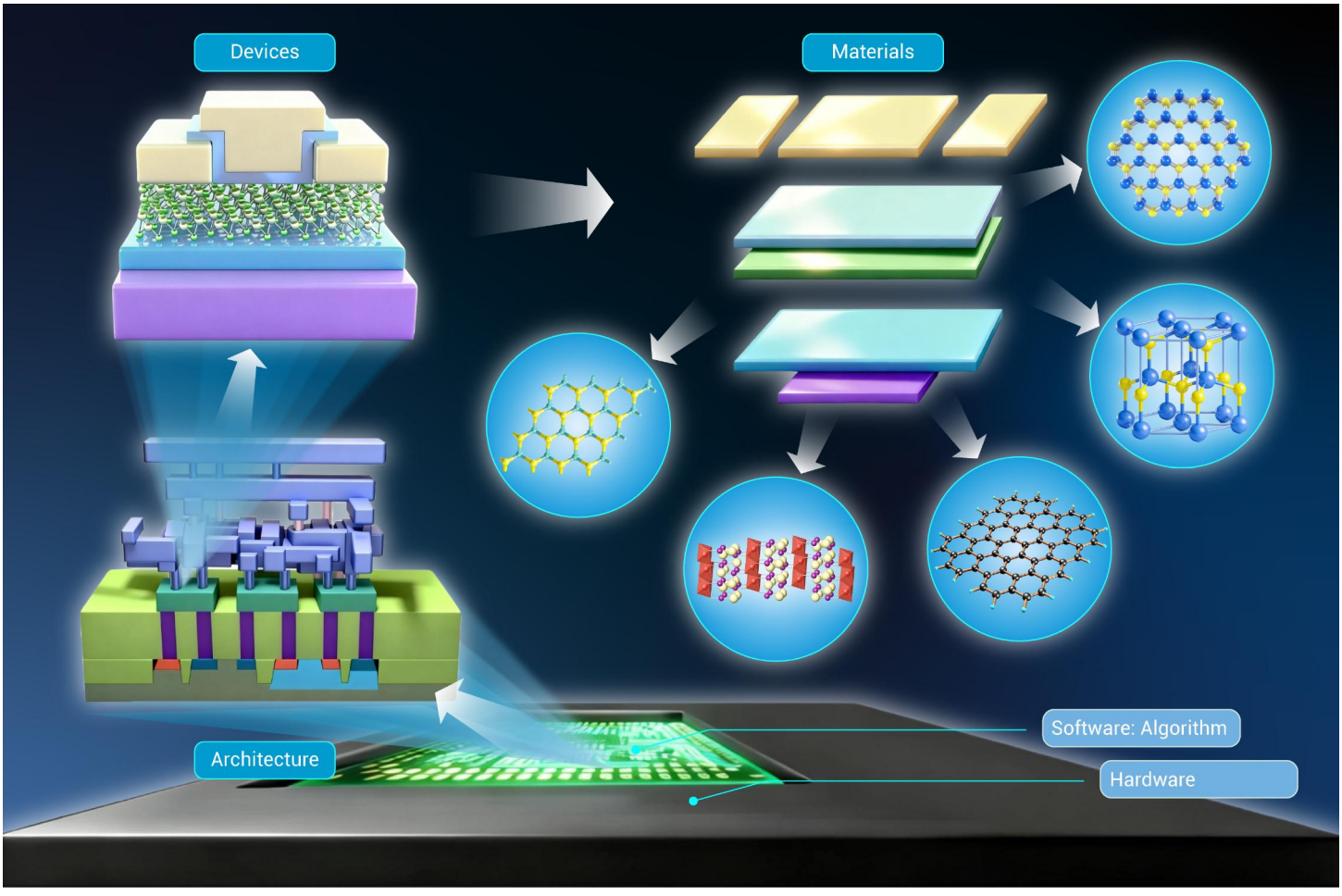

Figure 1. Development strategies for ICs This picture presents the collaborative development linkages among hardware including materials, devices formed with materials layer by layer, architectures built-up with devices including 3D packaging, encompassing the design process from fundamental materials to chip architectures, and software including algorithms and ideologies such as photonics/electronics hybrid applications.

provided such as efficient methods to take care of the defects introduced during the process, to develop the cost-effective synthesis of various 2D materials with controlled doping and quality, and to guarantee the scalable integration of contact, channel, and dielectric materials with industry compatibility and low contamination. These are believed to be some of the challenges of representative 2D materials.[1,3]

DEVICES

Translating material properties into practical performance depends critically on functional device design. In the case of devices, the multifunctional devices with compact structures and lab-fab process adaptability have been proposed, i.e.,MZT (multifunctional multi-terminal zero-additional-resistor-process one-transistor with the novel channel electrode design architecture) in AFM (DOI: 10.1002/adfm.202421204, patents CN 103178116, etc.). MZT is proved to be available to be fabricated in the Si foundry lines such as 55-nm complementary metal oxide semiconductor (CMOS) technology nodes and lab processes. MZT, with multi-terminals but no additional process to a standard transistor, can serve as logic gates which give out output voltages alone without adding a resistor, as a memory with 20-minute retention time, as an artificial synaptic device or as a sensor. The MZT logic NOT is found to be over 50% less than the CMOS logic NOT in the same foundry processing technology node. Given such performance and characteristics, it is not hard to tell that not only analog matrix computing (AMC) could be performed when using the devices as a memory unit,[4] but also logic gate computing could be performed using the devices in the same array. MZT devices are highly compatible with Si foundry processes. In summary, with MZT which could give both voltage and current outputs directly, a real computing-and-memory could be realized, because both the analog memory and logic gate computing could be performed in the same unit, similar to the brain function.

ARCHITECTURES

With high-performance devices as core building blocks, the system architectures built up by devices are also important, which could help to maximize device potential. While the von Neumann architectures are predominant presently, which separate data processing from memory, numerous other architectures have been explored, including 3D packaging/processing architectures and non-von Neumann designs like analog processing-in-memory arrays.[4] For instance, the resistive random-access memory (RRAM) chips have been proposed or involved for analog matrix equation solving. One analog matrix equation solver combines low-precision (LP) analog matrix inversion (INV) and high-precision (HP) analog matrix-vector multiplication (MVM): LP INV reduces iteration counts by delivering approximate results via closed-loop circuits, while HP MVM leverages slice matrices mapped to 1T1R TaO_x-based RRAM arrays.[4] At present, von Neumann architectures remain dominant because analog operations need to solve the variability, foundry compatibility and hence reliability challenges before wide applications.[2,3]

Another research highlights atomic device-to-chip (ATOM2CHIP) technology for modular 3D architectures.[3] This approach aims at alleviating emerging device incompatibility by creating specially-designed 2D-CMOS module interfaces and promoting 2D material applications in micro-level 3D packaging.[1,3] The yield is shown to be approximately 93.55%, lower than commercial IC yields due to challenges in integrating diverse processes, including 2D-CMOS, 2D-flash arrays, direct-writing lithography, transfer process, 3D packaging and so on. Consequently, validating mass-production yield stability and adapting lab-scale techniques to standard foundry workflows are critical prerequisites for unlocking the full potential of this technology in data-intensive processing ICs.[3]

ALGORITHMS

Software such as algorithms and ideologies plays a significant role in compensating for limitations induced by the hardware of materials, devices, and architectures (e.g., variability, scalability constraints, precision loss). This is particularly evident in memristor-based in-memory computing, where broad algorithmic development has been spurred by three general hardware challenges of memristor systems: intrinsic device non-idealities, insufficient input capacity, and system-level precision constraints.[5]

Addressing the first challenge of intrinsic device non-idealities, diverse algorithmic strategies have been catalyzed. Hardware-aware training is a widely adopted approach for alleviating pre-programming precision loss: by embedding device non-idealities as a noise layer in software training, it enhances the robustness of trained weights against hardware defects. For scenarios demanding precise weight programming, methods like write-verify programming have been proposed.[5]

Regarding the second challenge of insufficient input capacity, two primary solutions have been proposed. Blocked vector–matrix multiplication (VMM) splits large inputs and weight matrices into smaller sub-blocks to match the memristor array scale, while time-encoded VMM converts amplitude-based information into time-domain pulses. Both approaches have inherent drawbacks: blocked VMM introduces inter-block communication latency, and time-encoded VMM is highly sensitive to pulse encoding efficiency. Also, a number of pulse-based encoding schemes lack standard IC compatibility, limiting scalability. This reveals a presently notable gap status that current algorithms are often tailored to lab prototypes rather than industrial systems.[5]

Finally, common solutions to the third problem range from neural network quantization to hardware-software co-design for signal refinement. Moreover, diverse algorithmic adaptations have been developed for in-situ training—mixed-precision methods and the Manhattan Update Rule are established options, but new variants continue to emerge to balance precision, speed, and hardware compatibility.[5]

A multi-dimensional comparative framework is presented for evaluating four strategies-materials, devices (MZT), algorithms, and architecture-across six key performance dimensions, according to the IC main requirements and challenges (precision, energy efficiency, process compatibility, scalability, reliability). Each strategy plays a non-negligible role in addressing challenges; notably, MZT shows optimizable potential across all dimensions and thus is promising.

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DECLARATION OF INTERESTS

The authors declare no competing interests.